RF Power Reduction for CDMA/W-CDMA Cellular Phones

By controlling supply voltages for the RF power amplifier in a CDMA/W-CDMA cellular phone, you can improve the PA efficiency, minimize heat, and dramatically extend the phone's data/talk time.

To meet the stringent specifications for linearity and adjacent-channel power ratio (ACPR) found in the IS95/3GPP spread-spectrum standard, CDMA/W-CDMA[1] wireless handsets require highly linear Class-A or Class-AB RF power amplifiers. The power-added efficiency (PAE) for that type of PA, however, is only about 35% maximum at Po = 28dBm, and much lower for lower power levels.

The PA does not operate continuously in voice mode. When the phone user isn't speaking, it runs at half rate (50% of the time) or at one-eighth rate, so there is no worry about the phone heating up during voice mode. In data mode, however, the PA runs continuously until the data transmission is complete. The combination of low PA efficiency and continuous PA operation causes the battery to drain quickly, and the resulting internal power dissipation can also make the phone overheat.

Power dissipation was a major problem for the early W-CDMA handsets that supported high-speed data-transmission services. It forced designers to include larger area heat sinks, more airflow for cooling, and larger capacity (bigger) batteries. Had they not overcome the issue of power dissipation, today's handsets would be bulky and heavy. Fortunately, the past few years have alleviated this problem by providing a dramatic improvement in PA power efficiency for CDMA/W-CDMA cell phones.

How to Reduce PA Power?

In CDMA/W-CDMA systems, the PA's RF power output is not always at maximum. To optimize the cell capacity (number of simultaneous transmissions that a base station can handle), each mobile phone controls its RF output power such that the effective signal-to-noise level received at the base station is the same for each phone. A probability distribution of the RF output-power levels from many phones in a given area shows that the average output power from a typical CDMA/W-CDMA phone is about +10dBm for suburban conditions and about +5dBm for urban conditions. Thus, a useful target for improving PA efficiency is not the maximum power level, but an approximate range of +5dBm to +10dBm.

As shown in **Figure 1**, two supply voltages are required for the CDMA/W-CDMA power amplifier. V_{REF} provides bias for the internal driver and power-amplifier stages, and V_{CC} biases the collectors for the driver and power amplifiers. The PA supply current can be reduced by adjusting those two voltages.

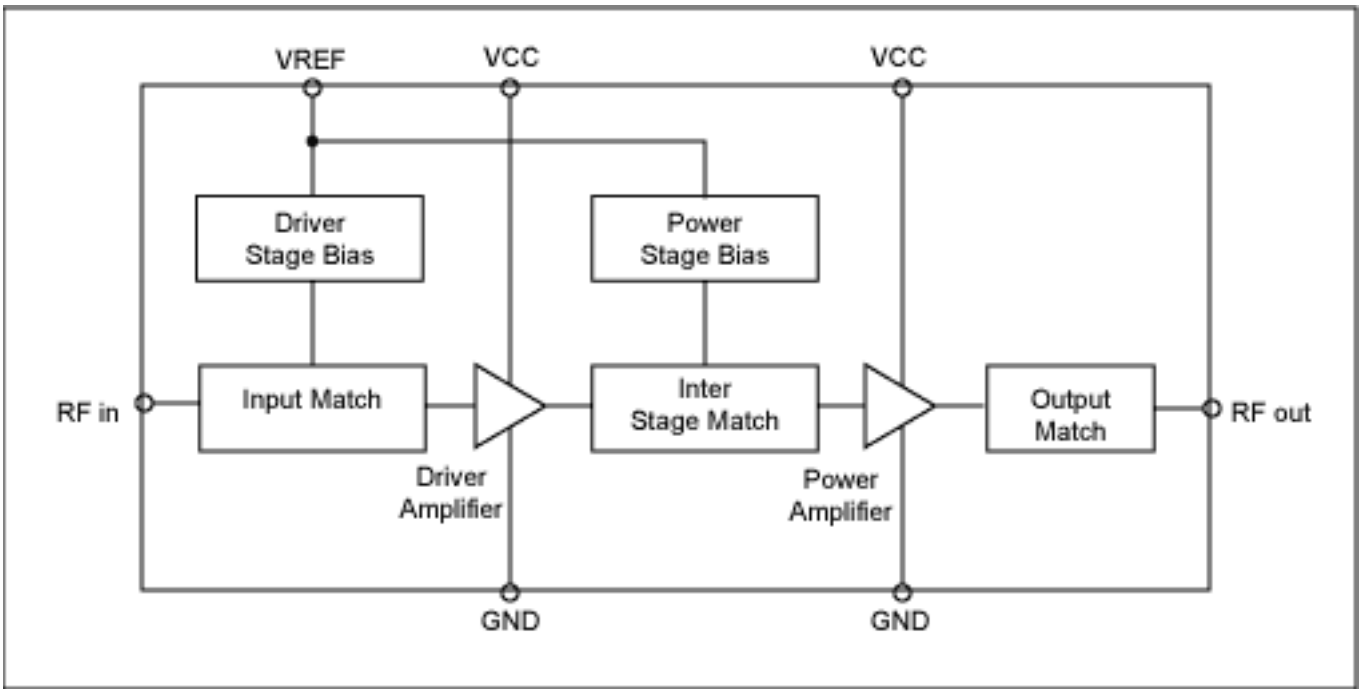

Figure 1. A typical power amplifier for CDMA/W-CDMA cell phones.

Reducing V_{REF}

When transmitting zero RF power, the PA itself draws a typical quiescent current of 100mA at V_{REF} = 3.0V and V_{CC} = 3.4V. Reducing V_{REF} from 3.0V to 2.9V causes the quiescent current to drop about 20mA. Thus, a dramatic savings can be achieved in PA quiescent current by lowering V_{REF}, but not below the point at which the PA linearity and ACPR begin to fail their specifications.

If there is experimental data giving the minimum V_{REF} voltage required to support each output-power level slotted for the PA, one can actively couple the control of V_{REF} with the PA's power-control process. If that approach is too difficult, one can simply implement a two-step change in V_{REF} that corresponds to the low-power mode (<10dBm) and high-power mode (>10dBm). To adjust V_{REF} via the baseband control DAC, use a low-power op amp with high output-current capability, along with an external gain setting.

Reducing the Collector-Bias Voltage

In typical wireless handsets, the PA V_{CC} is delivered directly from a single-cell Li-ion battery, resulting in an operating V_{CC} range of 3.2V to 4.2V. As mentioned above, statistics show that the CDMA/W-CDMA PA operates at power levels of +5dBm to +10dBm most of the time. At those levels one can reduce the PA collector bias voltage (V_{CC}) considerably without losing

linearity in the PA, and at the same time reduce the power loss from excessive collector-bias headroom. Based on experimental tests at low power levels, one can maintain proper communications with the base station while lowering the PA collector bias all the way down to 0.6V.

A variable bias voltage for the PA collector is provided by a specially designed, high-efficiency DC-DC stepdown converter. The output voltage of this converter is adjusted using a dedicated DAC output from the baseband processor.

DC-DC Converter Controls PA Power and PAE

The DC-DC converter controlling the PA collector voltage must respond quickly to a control signal. Usually, the converter's output voltage should settle to within 90% of its new target voltage within 30ms following a change in analog control voltage from the baseband processor. The converter chip provides an appropriate internal gain between its V_{CC}-control input and the output voltage that biases the PA collector. It also switches at high frequency, reducing the physical size of the inductor.

Connecting the DC-DC converter between the PA and battery highlights a problem—the demand for high RF power at low battery voltage. To deliver 28dBm RF power while maintaining the specification for PA linearity, PA manufacturers recommend a minimum V_{CC} of 3.4V. To maintain a 35% PAE at 3.4V, one also needs a high PA-collector current of 530mA:

28dBm RF power: $10^{2.8}$ mW = 631mW
Required PA power (V_{CC} x I_{CC}): 631mW/(PAE¤100) = 1803mW
Required PA I_{CC} at 3.4V V_{CC}: I_{CC} = 1803mW/3.4V = 530mA

To support a 3.4V V_{CC} and 530mA I_{CC}, the DC-DC converter for PA power requires a certain amount of input-to-output headroom. If, for example, on-resistance for the converter's internal p-channel MOSFET (P-FET) is 0.4Ω and the inductor resistance is 0.1Ω, the voltage drop across those two components in series will be (0.4Ω+0.1Ω) x530mA = 265mV. Thus, the DC-DC converter is unable to support a 3.4V output when the battery voltage drops below 3.665V.

In this case (battery voltage below 3.665V), it is better to short the PA collector to the battery. Otherwise, one cannot access the full capacity of the Li-ion battery. Normally, the solution is to bypass the inductor and internal P-FET by connecting a low-Rds(on) P-FET in parallel. This bypass P-FET (which can be internal or external) connects battery voltage directly to the PA collector when in the high-power mode (**Figure 2**). For the combination of high RF power and low battery voltage, this bypass measure is a must-do.

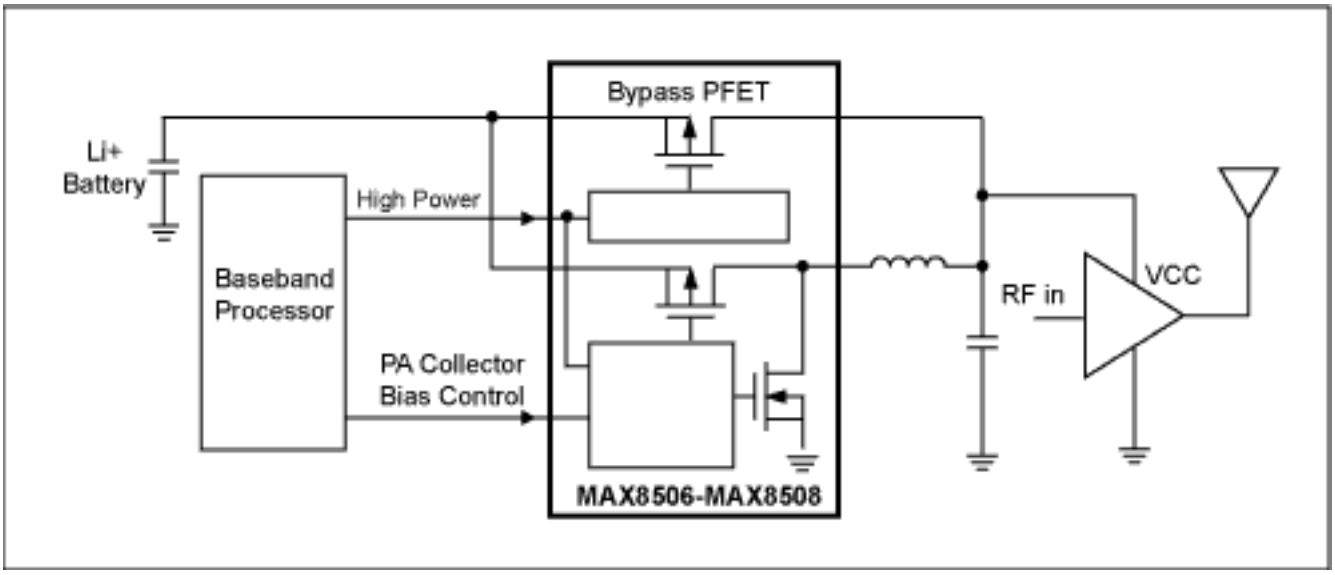

Figure 2. A DC-DC converter (middle IC) allows the baseband processor to exercise tight control over V_{CC} for the power amplifier.

The very best method for optimizing PAE is to adjust the PA-collector bias continuously. That approach, however, requires factory calibration and sophisticated software that ensures good PA linearity and ACPR in the presence of continuously changing collector bias. The next best approach is to change the bias level in a series of steps, usually two to four (**Figure 3**). A four-step system, for instance, might consist of V_{CC} values V_{batt}, 1.5V, 1.0V, and 0.6V. The overall efficiency in such a system is nearly as good as that for a system with continuous control of the PA collector bias, and for low- and mid-power levels the inductor needs only to support peak currents of less than 150mA.

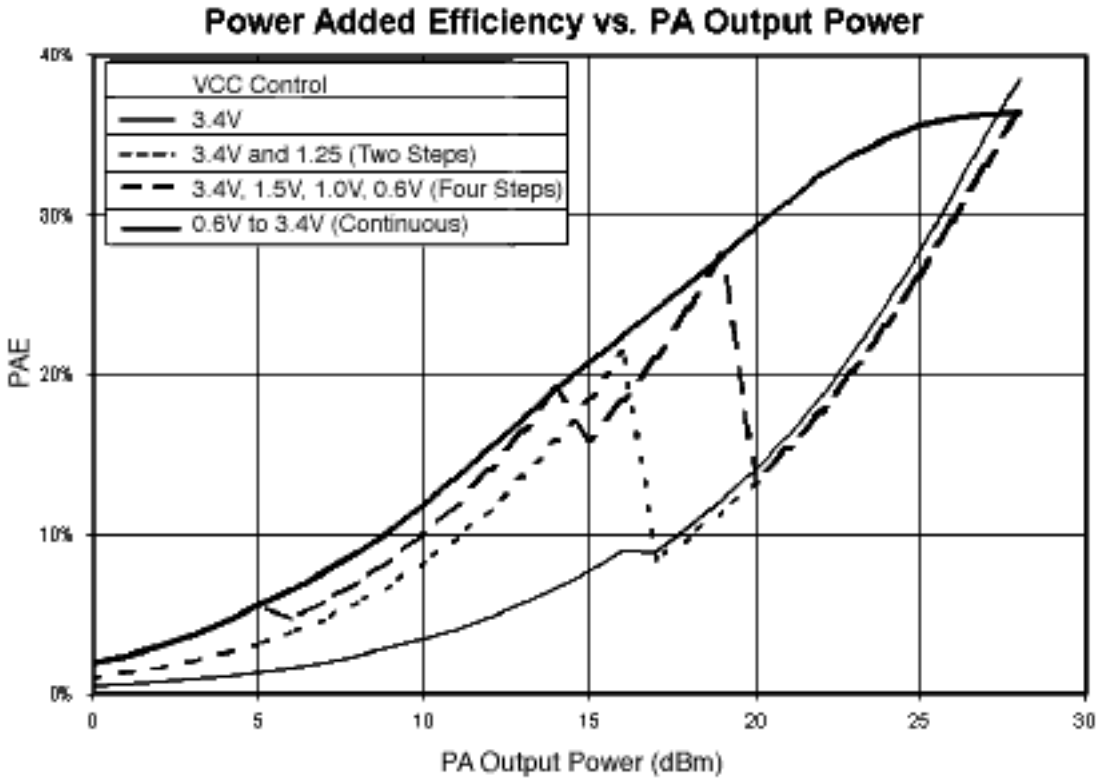

Figure 3. A DC-DC converter provides maximum power-added efficiency (PAE) for the power amplifier shown in Figure 2.

Notes

[1]Code Division Multiple Access/Wideband Code Division Multiple Access

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